Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (original) A power supply for a communication apparatus, comprising:

a source of a first control signal that is indicative when a first antenna signal is to be selected and when a second antenna signal is to be selected;

a power transistor responsive to said first control signal for generating an output supply voltage at a value selected, in accordance with said first control signal, said output supply voltage being coupled to a stage of said communication apparatus to select said first antenna signal, when a first value of said output supply voltage is generated and said second antenna signal, when a second value of said output supply voltage is generated;

a switch responsive to said first control signal and coupled to an input of said power transistor for selecting, in a first switching state of said switch, a first input supply voltage to be developed at said input, when said first antenna signal is selected, and, in a second switching state of said switch, a second input supply voltage to be developed at said input, when said second antenna signal is selected; and

a fault detector coupled to said switch for changing the switching state in said switch, when said second antenna signal is selected and a fault condition occurs, to select an input supply voltage to be developed at said input that is different from said second input supply voltage.

2. (original) The power supply according to Claim 1, wherein said output supply voltage is developed at a first main current conductive terminal of said power transistor and each of said first and second input supply voltages is selectively developed at a second main current conductive terminal of said power transistor to form a series pass regulator.

3. (original) The power supply according to Claim 2 wherein, in normal operation, when said first antenna signal is selected, a smaller magnitude of said output supply voltage is generated and said first input supply voltage having a smaller magnitude than said second input supply voltage is selected to be developed at said input of said power transistor in a manner to reduce a voltage difference between said first and second main current conductive terminals of said power transistor.

4. (original) The power supply according to Claim 2 wherein, in normal operation, when said second antenna signal is selected, a larger magnitude of said output supply voltage is generated and said second input supply voltage having a larger magnitude than said first input supply voltage is selected to be developed at said input of said power transistor and wherein, when said fault condition occurs, said first input supply voltage is selected instead of said second input supply voltage to be developed at said second main current conductive terminal of said power transistor to reduce a voltage difference between said first and second main current conductive terminals of said power transistor.

5. (original) The power supply according to Claim 2, further comprising a regulator coupled to said power transistor for regulating said output supply voltage in a negative feedback manner.

6. (original) The power supply according to Claim 1 wherein said fault detector comprises a comparator responsive to said output supply voltage for generating a second control signal that is coupled to said switch to change the switching state in said switch, when said output supply voltage is outside a normal operation range of values.

7. (original) The power supply according to Claim 6 wherein each of said first and second control signals is coupled to said switch via a stage performing a logic function.

8. (original) The power supply according to Claim 6 wherein said first control signal is generated in a microprocessor that is responsive to said second control signal.

9. (original) The power supply according to Claim 1 wherein said switch comprises a second transistor, wherein a power resistor is coupled between a pair of main current conductive terminals of said second transistor and wherein, when said second transistor is at a conductive switching state, said resistor is bypassed and a voltage that is developed at said input is higher than when said second transistor is at a non-conductive switching state and said resistor dissipates power.